REMARKS

The above Amendment and the following Remarks are in timely Reply to the non-final Office Action dated 01/02/03 in this Application. In light of this Reply, the Applicants respectfully request reconsideration and further examination of this Application, pursuant to 37 CFR 1.111.

Fifty-nine claims (1-59) were pending in this Application. In the above Amendment, seven claims (12, 13, 18, 26, 34, 43 and 54) were cancelled, and twenty claims (1, 10, 11, 16, 17, 23, 24, 28, 33, 35, 37, 38, 39, 41 and 44-49) were amended. Accordingly, 52 claims, of which six (1, 11, 17, 24, 41 and 49) are in independent form, remain pending in this Application for reconsideration and further examination.

In paragraph 4 of the Office Action, the Examiner rejected claims 1, 11, 17-18 and 21-23 under 35 U.S.C. 102(e) as being anticipated by Ellis et al. (U.S. Pat. 6,256,687), stating, in pertinent part,

> "a. As per ***claim 1***, Ellis discloses USB host system operationally coupled to a computing system with a main processor, comprising:
>
> ...
>
> - a communication area accessible both by the main processor and by the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in predefined formats.... (col.3, lines 35-67), (col. 4, lines 1-67), (col.5, lines 1-22)
>
> ...
>
> b. As per ***claim 11*** Ellis discloses a USB host system operationally coupled to a computing system, comprising:
>
> ...
>
> - an interface between (fig.2,170) the first processor and second processor that provides a high-level USB pipe view of a USB system to an application program running on the second processor in the computing system. (cot.5, lines 9-22)
>
> c. As per ***claim 17***, Ellis discloses an information processing system comprising:
>
> ...
>
> - a data transfer host system comprising a second processor implementing a first data transfer driver managing a data transfer between the said first processor and a device; a data transfer port for connecting a device to the said data transfer host system; and an interface with the first processor that provides a high-level view of the data transfer process to the first processor. (col. 3, lines 35-67), (col. 4, lines 1-67), (col. 5, lines 1-22), (col. 5, lines 9-22)" (Emphasis added)

In light of the above Amendments to independent claims 1, 11 and 17, and the Remarks that follow, this rejection is respectfully traversed.

Ellis et al. (the '687) describes a method and apparatus for managing data flow between a serial bus device that operates at a first data rate and a parallel port device that operates at a second data rate (Abstract). The '687 apparatus thus acts as a "translator" between a device having a

serial I/O interface, *e.g.*, a serial printer (Fig. 1, 172_k), and a device having a parallel I/O interface, *e.g.*, a PC (Fig. 1, 100), and includes a "communication area," *i.e.*, a buffer unit (Fig. 2, 240) that is accessible by both a "main processor" (Fig. 1, 110) and a "second processor," *i.e.*, a "receiver processor" (Fig. 3, 302) and a "transmitter processor" (Fig. 4, 402). However, an examination of Ellis et al. reveals that, unlike the present invention, the main processor 110 of Ellis et al. lacks a **direct** access to the communication area 240, and in particular, is via a series of "bridges" (Fig. 1, 120 and 145), which necessitate complicated "bus mastering" schemes, as well as a "parallel port interface circuit" (Fig. 2, 280; col. 4, lines 31-37) and a complex "control circuit" (Figs. 2 and 6, 250; col. 6, lines 26-51).

By contrast, the USB host system (Fig. 2, 200) of the present invention provides a **direct** access, *viz.*, via "a standard microprocessor bus interface 205," between the "communication area," *i.e.*, the "DCM" (Fig. 2, 220) and both the "main processor" (Fig. 3, 310; p. 8, lines 16-19) and the dedicated "second processor" (Fig. 2, 210). This results in a USB host system that does not rely on bus mastering techniques, thereby liberating the USB host system from PCs, processors and other platforms that utilize a PCI bus, and enabling a full-function USB host to be used in any embedded system using any application processor (p. 6, lines 5-5-10), and further, one that is both simpler and less expensive to implement. These distinctions between the Ellis et al. "translation" system and the true USB host system of the present invention are now more particularly pointed out and distinctly claimed by the respective recitations in amended independent claims 1, 11 and 17 of:

> **Claim 1**: "[A] communication area ***directly*** accessible by both the main processor and the first processor...."
>
> **Claim 11**: "[W]herein the interface comprises a memory that is ***directly*** accessed by both the first and second processors, and ***wherein the second processor interfaces with the host system via a standard micro-processor bus***.
>
> **Claim 17**: "[W]herein the interface comprises an area in a memory that is ***directly*** accessible by both the first processor and the second processor.

In light of the foregoing distinctions, it is respectfully submitted that the Examiner's rejection of claims 1, 11, 17-18 and 21-23 under 35 U.S.C. 102(e) in view of Ellis et al. (U.S. Pat. 6,256,687) is untenable and must be withdrawn.

In paragraph 5 of the Office Action, the Examiner rejected claims 24-32, 38-43 and 46-59 under 35 U.S.C. 102(d) as being anticipated by Larky et al. (U.S. Pat. No. 6,389,495), stating, in pertinent part,

> "a. As per ***claim 24***, Larky et al. discloses a USB host comprising:

- a first processor implementing a function of a USB system; (col. 4, lines 26-44)
- a downstream USB port; (fig.1,106)
- a memory accessible by the first processor and a second processor external to the USB host, ... (col.7, lines 21-67), (col.8, lines 1-18), (col.9, lines 26-35)

...

m. As per ***claim 41***, Larky discloses a USB host comprising:

- a first processor implementing a function of a USB system; (col.4, lines 22-44)
- a downstream USB port; (fig.1, 106)
- a memory accessible (fig.3, 104, 126) by both the first processor (fig 1, 116) and second processor(fig.1, 120) external to the said USB host, whereby the said second processor initiates a USB transfer by writing a transfer request, and data for the said transfer, if there is any, into a first area in the said memory, and the said first processor carries out the transfer, and writes the status of the said transfer, and data from the said transfer, if there is any, into a second area in the said memory. (col. 7, lines 21-67), (col.8, lines 1-18), (col.9, lines 26-35)

...

s. As per ***claim 49***, Larky discloses a USB host system operationally coupled to a computing system with a main processor, comprising a processor (fig. 1,120) that interfaces with the main processor (fig. 1, 116) via a communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a predefined record format and the processor schedules and completes the request via a USB host controller. (col.4, lines 26-44)

In light of the above Amendments to independent claims 24, 41 and 49, and the Remarks that follow, this rejection is respectfully traversed.

Larkey et al. (the '495) discusses a circuit for use in a control system of a USB peripheral device that is dedicated to tasks related to communication with a host computer implementing a USB host, such as the recognition and enumeration of the USB device without the use of the device's micro-controller (Abstract). However, Larkey et al. does not teach or even suggest the limitations of independent claims 24, 41 and 49, as amended herein, *viz.*:

Claim 24: "[A] a memory connected to both the first processor and a second processor external to the USB host ***via a standard microprocessor bus interface***...."

Claim 41: "[A] memory accessible by both the first processor and a second processor external to the USB host ***via a standard microprocessor bus interface*** ...."

Claim 49: "[W]herein the main processor and the processor are operationally coupled ***via a standard microprocessor bus interface***.

In light of the foregoing distinctions, it is respectfully submitted that the Examiner's rejection of claims 24-32, 38-43 and 46-59 under 35 U.S.C. 102(d) as being anticipated by Larky et al. (U.S. Pat. No. 6,389,495) is untenable, and must be withdrawn

In paragraph 7 of the Office Action, the Examiner rejected dependent claims 2-10 under 35 U.S.C. 103(a) as being unpatentable over Ellis et al. (the '687), above, as applied to independent claim 1 above, and further in view of Madden et al. (U.S. Pat. No. 6,393,493). This re-

jection is respectfully traversed on the grounds that Madden et al. does not supply the deficiencies in teaching of Ellis et al. discussed above in connection with independent claim 1. Thus, even if the suggested combination of the two references were to be made (for which there is no teaching or suggestion in either reference), the limitations of independent claims 2-10, which incorporate all the limitations of independent claim 1, would still not be met. Accordingly, the Examiner's rejection of claims 2-10 under 35 U.S.C. 103(a) over Ellis et al. (the '687) and further in view of Madden et al. (the '493) is untenable and must be withdrawn.

In paragraph 8 of the Office Action, the Examiner rejected dependent claims 12-16 under 35 U.S.C. 103(a) as being unpatentable over Ellis et al. (the '687), above, as applied to independent claim 11 above, and further in view of Madden et al. (the '493). This rejection is respectfully traversed on the grounds that Madden et al. does not supply the deficiencies in teaching of Ellis et al. discussed above in connection with independent claim 11. Thus, even if the suggested combination of the two references were to be made (for which there is no teaching or suggestion in either reference), the limitations of independent claims 12-16, which incorporate all the limitations of independent claim 11, would still not be met. Accordingly, the Examiner's rejection of claims 12-16 under 35 U.S.C. 103(a) over Ellis et al. (the '687) and further in view of Madden et al. (the '493) is untenable and must be withdrawn.

In paragraph 9 of the Office Action, the Examiner rejected dependent claims 19-20 under 35 U.S.C. 103(a) as being unpatentable over Ellis et al. (the '687), above, as applied to independent claim 17 above, and further in view of Mitra (U.S. Pat. No. 5,594,894). This rejection is respectfully traversed on the grounds that Mitra does not supply the deficiencies in teaching of Ellis et al. discussed above in connection with independent claim 17. Thus, even if the suggested combination of the two references were to be made (for which there is no teaching or suggestion in either reference), the limitations of independent claims 19-20, which incorporate all of the limitations of independent claim 17, would still not be met. Accordingly, the Examiner's rejection of claims 19-20 under 35 U.S.C. 103(a) over Ellis et al. (the '687) and further in view of Mitra (the '894) is untenable and must be withdrawn.

The Applicants do not understand the Examiner's comments beginning the second paragraph of page 13 of the Office Action, and accordingly, are unable to reply to them herein.

WHEREFORE, each and every objection and rejection of the Office Action of 01/02/03 having been fully addressed and overcome herein, it is respectfully submitted that this Applica-

tion, including now-pending claims 1-11, 14-17, 19-25, 27-33, 35-42, 44-53 and 55-59, is now in a condition for Allowance. An early Notice thereof is therefore earnestly solicited by the Applicants.

Respectfully submitted,

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ATTACHMENT A

In the claims:

In the following amendments, deletions are shown **[bold and enclosed in brackets]**, and insertions are shown **bold and underlined**.

claims 1, 10, 11, 16, 17, 23, 24, 28, 33, 35, 37, 38, 39, 41 and 44-49 are amended as follows:

1. (Twice amended) A USB host system operationally coupled to a computing system with a main processor, comprising:

a first processor that implements a USB driver without using the main processor resources;

a downstream USB port; **and,**

a communication area **directly** accessible **by** both **[by]** the main processor and **[by]** the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats,

wherein the main processor writes a data transfer request in the communication area in a pre-defined record format, and

wherein the first processor schedules and completes the request via a USB host controller.

10. (Twice amended) The USB host system of claim 1, wherein **the second processor runs an operating system supporting USB, and** the USB host system **[is used to]** provides a USB host function to the **[said]** second processor **[which runs an operating system supporting USB,]** by intercepting calls to a USB driver in the operating system.

11. (Twice amended) A USB host system operationally coupled to a computing system, comprising:

a first processor implementing a function for managing a USB host controller with or without an operating system running on the computing system;

a down stream USB port; **and,**

an interface between the first processor and a second processor that provides a high-level USB pipe view of a USB system to an application program running on the second processor in the computing system,

wherein the interface comprises a memory that is directly accessed by both the first and second processors, and

wherein the second processor interfaces with the host system via a standard microprocessor bus.

16. (Amended) The USB host system in claim **[1] 11** where**in the second processor runs an operating system supporting a USBD, [said]**

wherein the host system **[is used to]** provide**s** a USB host function to the **[said]** second processor**, including a USBD function** [which runs an operating system supporting a USBD], and

wherein the host system processes a USB transfer request by the **[said]** second processor **by** intercepting calls to the USBD in the **[said]** operating system **and passing the calls to the USBD in the host system**.

17. (Amended) An information processing system comprising:

a first processor; **[and]**

a data transfer host system comprising a second processor implementing a first data transfer driver managing a data transfer between the **[said]** first processor and a device;

a data transfer port for connecting **[a] the** device to the **[said]** data transfer host system; and,

an interface **between the host system and [with]** the first processor that provides a high-level view of the data transfer process to the first processor,

wherein the interface comprises an area in a memory that is directly accessible by both the first processor and the second processor.

23. (Amended) The information processing system of claim 17, wherein the **[said]** first processor contains a second data transfer driver capable of managing the **[same said]** data transfer, and **wherein** a data transfer request by the **[said]** first processor to the **[said]** second data transfer driver is carried out by the **[said]** data transfer host system.

24. (Twice amended) A USB host comprising:

a first processor implementing a function of a USB system;

a downstream USB port; and

a memory **connected to both** **[accessible by]** the first processor and a second processor external to the USB host **via a standard microprocessor bus interface**,

wherein a first area of the memory with **a** first predetermined format is used for a first type of transfer, and a second area of the memory with a second predetermined format is used for a second type of transfer.

28. (Amended) The **USB host of** **[third area of the storage device in]** claim 27, wherein the **[said]** third area is in a part of the **[said]** memory **that** **[which]** is read-only to the second processor.

33. (Amended) The USB host of claim 24, wherein the **respective** starting addresses of the first **and second** areas **are at** **[can be in]** different **locations in** **[part of]** the memory.

35. (Amended) The USB host of claim 24, wherein the **respective** starting addresses of the **[said]** first and second areas are **at** [in] the same location **in** **[of]** the memory.

37. (Amended) The USB host of claim 24, wherein the **respective** starting addresses of the **[said]** first and second areas are stored at fixed locations **in** **[of]** the memory.

38. (Amended) The USB host of claim 24, wherein the second processor writes a transfer request in **one of** [a] said areas in the memory and notifies the first processor **of the request** with an interrupt signal.

39. (Amended) The USB host of claim 24, wherein the first processor writes the status or data of a transfer into **one of** **[a]** said areas in the memory and notifies the **[said]** second processor **of the request** with an interrupt signal.

41. (Amended) A USB host comprising:

a first processor implementing a function of a USB system;

a downstream USB port; and,

a memory accessible by both the **[said]** first processor and a second processor external to the **[said]** USB host **via a standard microprocessor bus interface**,

wherein **[whereby]** the **[said]** second processor initiates a USB transfer by writing a transfer request**[,]** and **any** data **to be transferred** [for the said transfer, if there is any,] into a first area in the **[said]** memory, and

wherein the **[said]** first processor carries out the transfer**[,]** and writes the status of the **[said]** transfer**[,]** and **any transferred** data [from the said transfer, if there is any,] into a second area in the **[said]** memory.

44. (Amended) The USB host **of** **[in]** claim 41, wherein the **[said]** first **and second** areas in the **[said]** memory **[and the said second area in the said memory]** are the same area.

45. (Amended) The USB host **of** **[in]** claim 41, wherein the **[said]** first **and second** areas in the **[said]** memory **[and the said second area in the said memory]** use **the** **[a]** same predefined format.

46. (Amended) The USB host of claim 41, wherein the second processor runs an operating system that supports **a** USB **driver,** and **wherein a** USB transfer request **initiated** by the **[said]** second processor to **the** USB driver **[on the second processor on the second processor]** is carried out by the USB host.

47. (Amended) The USB host of claim 41, wherein **[when the said first processor carries out the transfer, and writes the status of the said transfer, and data from the said transfer, if there is any, into a second area in the said memory,]** the **[said]** USB host **transmits** [generates] an interrupt signal to the [said] second processor to notify the **[said]** second processor **that the transfer has been completed**.

48. (Amended) The USB host of claim 41, wherein **[when the said second processor initiates a USB transfer by writing a transfer request, and data for the said transfer, if there is any, into a first area in the said memory,]** the **[said]** second processor **transmits** **[generates]** an interrupt signal to the **[said]** USB host to notify the **[said]** USB host **that the second processor has initiated a USB transfer**.

49. (Amended) A USB host system operationally coupled to a computing system with a main processor, comprising:

a processor that interfaces with the main processor via a communication area using pre-defined records in pre-defined formats,

wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the processor schedules and completes the request via a USB host controller**, and**

wherein the main processor and the processor are operationally coupled via a standard microprocessor bus interface.